A Multichannel Femtoampere-Sensitivity Potentiostat Array for Biosensing Applications

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***Abstract*—Rapid and accurate detection of pathogens using conductometric biosensors requires potentiostats that can measure small variations in conductance. In this paper, we present an architecture and implementation of a multichannel potentiostat array based on a novel semi-synchronous sigma–delta ($\Sigma\Delta$) analog-to-digital conversion algorithm. The algorithm combines continuous time $\Sigma\Delta$ with time-encoding machines, and enables measurement of currents down to femtoampere range. A 3-mm $\times$ 3-mm chip implementing a 42-channel potentiostat array has been prototyped in a 0.5-μm CMOS technology. Measured results demonstrate that the prototype can achieve 10 bits of resolution, with a sensitivity down to 50-fA current. The power consumption of the potentiostat has been measured to be 11 μW per channel for a sampling rate of 250 kHz. Experiments with a conductometric biosensor specific to *Bacillus Cereus* bacterium, demonstrate the ability of the potentiostat in identifying different concentration levels of the pathogen in a biological sample.**

***Index Terms*—Analog-to-digital (A/D) converter, asynchronous sigma–delta ($\Sigma\Delta$) converter, biosensors, current-mode $\Sigma\Delta$ converter, femtoampere current measurements, multichannel converter, potentiostat.**

I. Introduction

BIOSENSORS have emerged as a promising technology for rapid detection of pathogens with applications in homeland security and medicine. [1]. The general function of a biosensor is to transduce binding events between biological receptors and target agents into a quantifiable electrical signal [3], [4]. Current research in biosensor technology has been towards developing better transducers that demonstrate superior sensitivity, portability, accuracy and throughput. Immunosensors (biosensors that use antibodies as receptors) are of great interest because of their applicability (any compound can be analyzed as long as specific antibodies are available), specificity (selectivity of antigen-antibody reaction) and high sensitivity. We had previously reported an antibody-based immunosensor [5] that used polyaniline based nanowires to transduce binding events between pathogens and their target antibodies into change in conductance. The sensor was successfully demonstrated for detecting *E. Coli* [5] and *bovine viral diarrhea virus* [6] and its sensitivity was reported to be 80 colony forming units per milliliter (CFU/ml), with a response time of less than 10 min. However, trace detection (detecting ultra-low concentration) of pathogens using the conductometric biosensor requires accurate and miniaturized current measurement circuits that can be integrated in proximity to the biosensor.

In this paper, we propose a novel multichannel potentiostat array that can demonstrate a detection range of up to femtoamperes of current, and hence can be used for measuring small changes in conductance. In literature, several multichannel potentiostats and current-mode data converters have been proposed for electrochemical measurements. For instance, in [8], [9], a $\Sigma\Delta$ approach was used for measuring currents generated due to neurochemical reactions. An integrating analog-to-digital (A/D) conversion technique was used in [10] for cyclic voltammetery based measurements and was demonstrated for sensitivity up to picoamperes of current. Integrated and implantable potentiostats have been reported for glucose concentration measurement with accuracy of nanoamperes [11].

However, for measuring currents in the range of sub-picoamperes, noise due to charge injection and substrate coupling becomes a limiting factor. Other source of interference include fundamental noise that limit the resolution of current measurements [12]. One possible solution to alleviate the effect of thermal noise is to use larger integration time in current-mode $\Sigma\Delta$ converters as has been proposed in [8]. Increase in integration time, however, reduces the speed of A/D conversion. In this paper, we present an alternative method called *semi-synchronous* $\Sigma\Delta$ modulation that can achieve current sensitivity range of up to femtoamperes without significantly reducing the conversion rate. The proposed architecture uses a novel semi-synchronous $\Sigma\Delta$ modulation technique that combines asynchronous time-encoding machine (TEM) proposed in [13] with a continuous time $\Sigma\Delta$ ($\mathrm{CT}\Sigma\Delta$) conversion [14]. For measurement of large magnitude currents, the operation of semi-synchronous $\Sigma\Delta$ converter is determined by $\mathrm{CT}\Sigma\Delta$ modulation, whereas for measurement of small input currents the operation is dominated by TEM. As will be shown in Section IV, that this combination improves robustness of current measurements to noise robustness especially for ultra-low currents.

This paper is organized as follows. Section II describes the semi-synchronous $\Sigma\Delta$ modulation and compares it with a conventional continuous time $\Sigma\Delta$ converter. Section III describes the circuit implementation of the $\Sigma\Delta$ modulator. Section IV analyzes the noise performance of the proposed converter. Section V describes some of the measured characteristics obtained using the fabricated prototype. Section VI uses the potentiostat chip to measure the response of a biosensor and Section VII provides conclusions with future directions.

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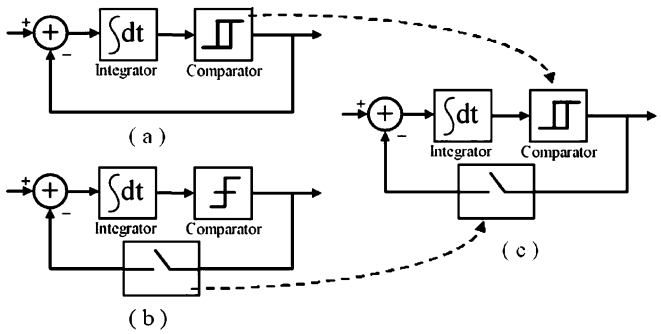

Fig. 1. Architecture of a (a) time-encoded modulation (TEM) (b) continuous time $\Sigma\Delta$ (c) semi-synchronous $\Sigma\Delta$ converter.

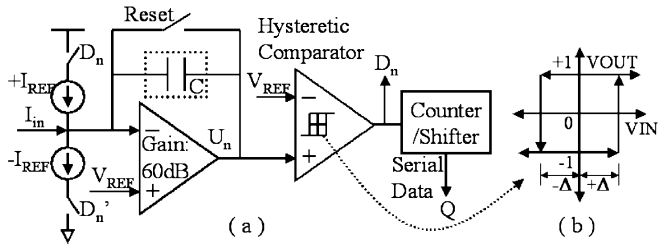

Fig. 2. Architecture of the proposed semi-synchronous $\Sigma\Delta$ converter. D_n' denotes the complement of D_n.

II. Semi-Synchronous $\Sigma\Delta$ Algorithm

The architecture of the proposed semi-synchronous $\Sigma\Delta$ potentiostat is shown in Fig. 1(c) and is compared with a TEM [Fig. 1(a)] and a continuous time $\Sigma\Delta$ based converters [Fig. 1(b)]. A TEM topology uses an integrator and a hysteretic comparator in a feedback configuration [see Fig. 1(a)] to produce a pulsewidth-modulated (PWM) digital sequence whose duty cycle is controlled by input signal. TEM encoding has been extensively studied in literature and readers are referred to [15], [13] for details. In [15], a sampling stage was added outside the TEM feedback loop which led to an asynchronous $\Sigma\Delta$ architecture. CT$\Sigma\Delta$ technique as shown in Fig. 1(b) uses a nonhysteretic comparator and a sampling stage inside the feedback loop. The CT$\Sigma\Delta$ topology has been applied for designing potentiostats that can measure up to pico-amperes of current [8]. The proposed semi-synchronous $\Sigma\Delta$ converter combines these two techniques by using a hysteretic comparator and a sampling stage in a feedback loop, which is shown in Fig. 1(c). As will be shown in the following description, that addition of comparator hysteresis reduces the converter switching cycles when operating with small magnitude currents. This leads to reduction in substrate noise interference and improves linearity of the converter by reducing the number of switching operations on reference current sources.

In this section, a time-domain analysis of a first-order semi-synchronous $\Sigma\Delta$ modulation is presented and is based on schematic shown in Fig. 2(a). The semi-synchronous algorithm consists of a synchronous conversion step which is equivalent to CT$\Sigma\Delta$ procedure, followed by an asynchronous compensation step which is equivalent to TEM.

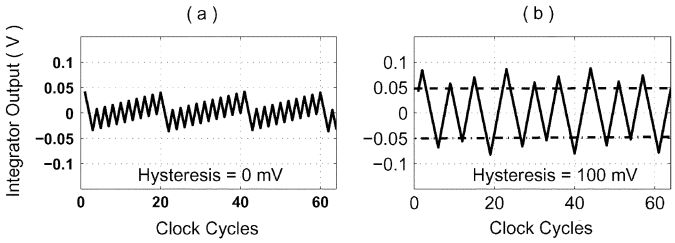

Fig. 3. Comparison of integrator output at different hysteresis levels (a) 0 V and (b) 100 mV.

A. Synchronous Conversion

Similar to analysis of most $\Sigma\Delta$ based potentiostats [8], the bandwidth of the input signal (current) will be assumed to be much less compared to the sampling frequency. Therefore, the time-domain analysis can be simplified by considering only a DC input current, which will be denoted by $I_{\rm in}$. During the synchronous conversion step, a combination of input current and a reference current $(I_{\rm ref})$ is first integrated on a capacitor [shown in Fig. 2(a)] for every clock cycle. The output of the integrator will be denoted by U_n and the index of clock cycles will be denoted by $n = 1,\ldots,N$. The integrated voltage is then compared against a reference voltage $V_{\rm ref}$ using a hysteretic comparator whose input-output response is shown in Fig. 2(b). We will denote the hysteresis level by Δ and the output of the comparator will be denoted by $D_n \in \{-1,+1\}$, that is used for triggering positive and negative reference currents $I_{\rm ref}$ [see Fig. 2(a)]. During each clock cycle n, the integrator voltage U_n is updated according to

$$U_n = U_{n-1} + \left(\frac{I_{\rm in}}{I_{\rm Ref}} - D_n\right)\frac{I_{\rm Ref}T_{\rm CLK}}{C} \tag{1}$$

$$D_n = \text{sign}(U_{n-1} + D_{n-1}\Delta) \tag{2}$$

where $\text{sign}(\cdot) \in \{+1,-1\}$ denotes a signum operator implementing the comparator, $T_{\rm CLK}$ denotes the duration of each clock cycle and C denotes the integrating capacitance. Compared with CT$\Sigma\Delta$ operation [8], the digital output D_n in (1) is correlated with digital outputs at previous clock cycles and is controlled by hysteresis level of the comparator Δ. Even though a general treatment of the proposed semi-synchronous $\Sigma\Delta$ would include dynamic modulation of hysteresis level, for the purposes of this paper, this level will be fixed to a constant value Δ. This ensures that the integrator voltage satisfies $|U_n| > \Delta$ before the output of the comparator switches. This effect is illustrated in Fig. 3, which shows the output of the integrator for different hysteresis levels. For sufficiently low magnitude of $I_{\rm ref}T{\rm clk}/C \gg \Delta$, the integrator output exhibits significantly higher switching cycles [see Fig. 3(a)] as compared to a converter operating with a larger magnitude of Δ [see Fig. 3(b)]. The reduction in switching cycles also reduces substrate noise and integrator nonlinearity which are important for measurement of ultra-low magnitude input currents.

Using recursion (1), it can be shown that the integrator output U_n in (1) is bounded according to

$$|U_n| \le \Delta + \frac{2I_{\rm Ref}T_{\rm CLK}}{C}. \tag{3}$$

When compared to an equivalent CT$\Sigma\Delta$, the response of the integrator is amplified, which degrades the resolution of the proposed conversion algorithm (due to larger value of residue). We will now show that the effect of this amplification can be utilized by an extended counting step that will enhance the resolution of semi-synchronous converter by 1 bit over a conventional $\Sigma\Delta$ converter, without incurring significant penalties in conversion rate. The recursion (2) can be rewritten in terms of auxiliary variables $V_n = U_n + D_n\Delta$ as

$$V_n = V_{n-1} + \left(\frac{I_{\text{in}}}{I_{\text{Ref}}} - D_n\right)\frac{I_{\text{Ref}}T_{\text{CLK}}}{C} + (D_n - D_{n-1})\Delta. \tag{4}$$

The recursion (4) can be seen to be composed of a $\Sigma\Delta$ step and a hysteretic modulation step that determines the correlation between consecutive digital bits. After N clock cycles, the recursion (4) yields

$$\frac{V_N}{N} = \left(\frac{I_{\text{in}}}{I_{\text{Ref}}} - \frac{1}{N}\sum_{n=1}^{N} D_n\right)\frac{I_{\text{Ref}}T_{\text{CLK}}}{C}l + \frac{(D_N - D_0)\Delta}{N}. \tag{5}$$

Thus, the residue V_N of a semi-synchronous $\Sigma\Delta$ conversion is a combination of residue due to a conventional $\Sigma\Delta$ conversion and a hysteretic residue $H_N = ((D_N - D_0)\Delta)/(N)$. A compensation step is therefore required to alleviate the degradation in resolution due to residue amplification and hysteresis.

B. Compensation Step

The compensation step is similar to extended counting technique [16] and is used for enhancing the resolution of a $\Sigma\Delta$ converter. Even though several extended counting algorithms could be used for compensation, in this paper, an asynchronous integrating A/D conversion has been used. At the start of this procedure, the input current I_{in} is disconnected and the reference current is allowed to charge (discharge) the voltage stored on the integrating capacitor (see Fig. 4). If the output of the comparator during the compensation steps is denoted by D_n^*, and the output of integrator is denoted by U_n^*, then at each cycle of compensation steps the integrator output is given by

$$U_n^* = U_{n-1}^* - D_n^*\frac{I_{\text{Ref}}T_{\text{CLK}}}{C} \tag{6}$$

with $U_0^* = U_N$. As shown in Fig. 4, the compensation step governed by (6) is applied till the integrator voltage U_n^* reaches or exceeds the hysteresis level Δ (see Fig. 4). This condition is inferred by monitoring the output of the comparator and is flagged for n where $D_n^* = -1, D_{n-1}^* = 1$. Also, by ensuring that the initial condition $D_0 = -1$, the error due to hysteretic residue in (5) is eliminated. Combining (5) and (6), the integrator output after N synchronous and N_{ext} asynchronous conversion cycles can be written as

$$\Delta + \epsilon = \left(N\frac{I_{\text{in}}}{I_{\text{Ref}}} - \sum_{n=1}^{N} D_n - \sum_{n=1}^{N_{\text{ext}}} D_n^*\right)\frac{I_{\text{Ref}}T_{\text{CLK}}}{C} \tag{7}$$

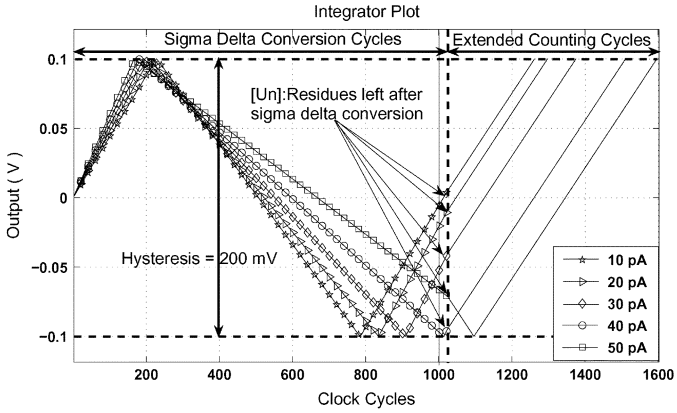

Fig. 4. Illustration of compensation step for the semi-synchronous $\Sigma\Delta$ conversion. The residue at the end of synchronous conversion is discharged (charged) using a reference current to a reference potential Δ.

where ϵ is the error incurred in determining the condition when the integrator output is $U_{N_{\text{ext}}}^* = \Delta$. Equation (7) can be re-written as

$$\frac{1}{N}\left(\sum_{n=1}^{N} D_n + \sum_{n=1}^{N_{\text{ext}}} D_n^*\right) = \frac{I_{\text{in}}}{I_{\text{ref}}} - \frac{\Delta}{\alpha N} - \frac{\epsilon}{\alpha N} \tag{8}$$

where $\alpha = I_{\text{ref}}T_{\text{CLK}}/C$. Equation (8) states that the synchronous conversion cycles reduces the error incurred during the asynchronous compensation step as ϵ/N. The magnitude of the final residue after compensation can be verified to be bounded by $|\epsilon| < I_{\text{ref}}T_{\text{clk}}/C$ which is half the error obtained when using a conventional $\Sigma\Delta$ [14]. Thus, a semi-synchronous $\Sigma\Delta$ converter with a compensation step provides an extra bit of resolution over a conventional $\Sigma\Delta$ converter.

III. Circuit Implementation

Fig. 5 shows the circuit level implementation of sub-systems in schematic 2. A standard folded cascode op-amp shown in Fig. 5(a) has been used to implement the integrator that provides 60-dB open-loop gain. As opposed to cascoded inverter based implementation [8], the differential amplifier based implementation can achieve a symmetrical and larger integration range about the reference potential. A digitally programmable capacitor bank has been used for the implementation and allows adjustable integration gain according to the (1). The hysteretic comparator shown in Fig. 5(b) is implemented using basic differential pair with current starved inverters. The positive hysteresis level $+\Delta$ and the negative hysteresis level $-\Delta$ can be programmed based on the range of input current and are also determined by ambient noise level of the integrator. Cascoded current sources and sinks have been used for implementing reference current generation. The multiplication between the digital bit D_n and I_{ref} according to (1) is implemented by switching (on/off) the cascoded current sources (sink) at the source (see Fig. 2). Switching at the source as opposed to switching at the drain has several advantages [17] as it reduces channel charge injection [17] and clock feed-through at the integration node. The low-pass filtering (counting) of comparator bits is performed using a 16-bit current starved counter/shifter. The circuit implementation uses building blocks that have been

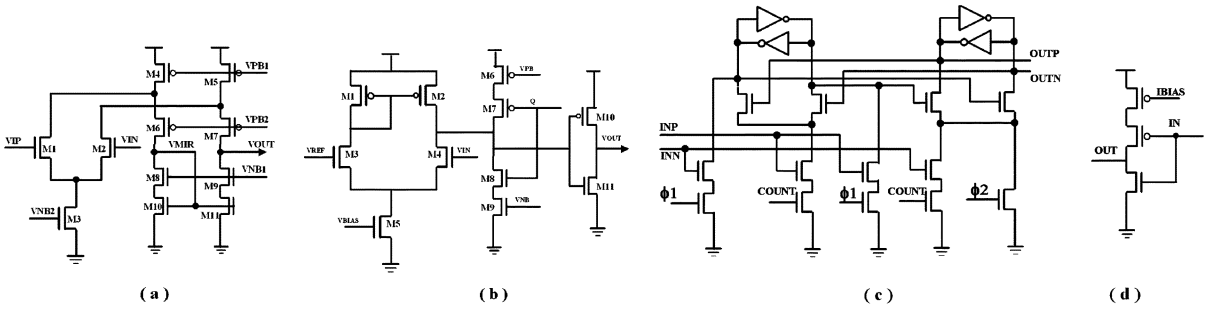

Fig. 5. (a) Folded cascode op-amp used for implementing the integrator. (b) Schematic diagram of hysteretic comparator. (c) Schematic of the counter/shift register cell. (d) Current starved inverter used in counter/shifter.

reported in [18]. Fig. 5(c) shows a single bit implementation of a counter/shifter and operates as one bit counter and shifter. This configuration leads to implementation which is compact and consumes less power. The circuit consists of two latches and an nMOS network that implements the counter/shifter logic. Current starved latches have been used based on inverters shown in Fig. 5(d), which provides a better control over frequency and power consumption of the counter/shifter. In count mode, two latches are cross coupled by activating the signal COUNT and deactivating the signals ϕ_1 and ϕ_2. In shift mode, the signal COUNT is set to low, and two nonoverlapping clock signals are used at ϕ_1 and ϕ_2 to shift the signal for readout. The counter/shifter architecture allows several stages to be daisy chained, which ensures scalable serial read-out architecture for multichannel potentiostats.

IV. Noise Analysis and Performance Limitations

Several factors limit the performance of the proposed semi-synchronous $\Sigma\Delta$ converter which includes finite gain of operational amplifier, comparator delay, offset and thermal noise. Finite gain, comparator delay and offset affect the performance of semi-synchronous converter in a similar fashion as conventional $\mathrm{CT}\Sigma\Delta$ converter. Therefore, in this section, we analyze the effect of thermal noise on the performance of semi-synchronous $\Sigma\Delta$ converter and illustrate benefits of using a hysteretic comparator for low current measurements. We will only consider the case where the input current $I_{\mathrm{in}} = 0$ and the integration capacitance C in Fig. 2 is being charged and discharged by only reference currents I_{ref}. The thermal noise contribution due to current references and the operational amplifier, can be summarized as a single equation according to [19], [20]

$$I_N^2(f) = 4\gamma KTg_{m_{\mathrm{eq}}}\Delta f \tag{9}$$

where K is Boltzmann's constant, T is absolute temperature, and $g_{m_{\mathrm{eq}}}$ is the equivalent conductance that combines effects of input referred noise due to current references and operational amplifier. Δf denotes the bandwidth of the converter, and $\gamma = 2/3$ for above-threshold operation and $\gamma = 1/2\kappa$ for subthreshold operation. The $1/f$ noise can be modeled as an offset in the reference current whose effect on any $\Sigma\Delta$ converter is minimal (provided the integrator does not saturate). For zero input current, the transition points of the integrator output are marked by events where the hysteretic comparator changes its state (comparator switching cycle). The total integration time between two comparator events can be approximated by

$$T_{\mathrm{int}} = 2\left(\frac{C\Delta}{I_{\mathrm{ref}}T_{\mathrm{clk}}} + 1\right)T_{\mathrm{clk}}. \tag{10}$$

The additive factor accounts for a $\Sigma\Delta$ step superimposed on a TEM step. The reference current noise is integrated to obtain an equivalent voltage noise whose signal power is given by

$$V_n^2 = \left(I_n^2\right)\left(T_{\mathrm{int}}/C\right)^2. \tag{11}$$

Even though the integration period is finite and requires a $\mathrm{Sinc}^2()$ factor for computing the bandwidth Δf, for the sake of simplicity, Δf is approximated by $1/T_{\mathrm{int}}$ which leads to total noise power of

$$V_n^2 \approx \frac{8KT\gamma g_{m_{\mathrm{eq}}}}{C^2}\left(\frac{C\Delta}{I_{\mathrm{ref}}T_{\mathrm{CLK}}} + 1\right)T_{\mathrm{CLK}}. \tag{12}$$

The signal power is given by the square of the integrated voltage and is at the output of an integrator

$$V_{\mathrm{sig}}^2 \approx \left(\frac{I_{\mathrm{ref}}T_{\mathrm{int}}}{C}\right)^2. \tag{13}$$

From (10)–(13), the signal-to-noise ratio (SNR) per integration cycle is computed as

$$\frac{V_{\mathrm{sig}}^2}{V_n^2} = \frac{I_{\mathrm{ref}}^2T_{\mathrm{CLK}}}{8KT\gamma g_{m_{\mathrm{eq}}}}\left(\frac{C_{\mathrm{int}}\Delta}{I_{\mathrm{ref}}T_{\mathrm{CLK}}} + 1\right) \tag{14}$$

For small values of reference currents, transistors in current references and amplifiers can be biased in weak inversion, where the equivalent transconductance $g_{m_{\mathrm{eq}}} = \kappa/U_T(I_{\mathrm{ref}} + I_{\mathrm{bias}})$, with I_{bias} being the tail current of the operational amplifier. Substituting values of $\gamma = 1/2\kappa$ for weak-inversion and thermal voltage $U_T = KT/e$ into (14), the SNR achieved during a single comparator switching cycle is given by

$$\frac{V_{\mathrm{sig}}^2}{V_n^2} = \frac{C\Delta U_T}{8\eta KT} + \frac{I_{\mathrm{ref}}T_{\mathrm{clk}}U_T}{8\eta KT} \tag{15}$$

where $\eta = (1 + I_{\mathrm{bias}}/I_{\mathrm{ref}})$. The SNR consists of thermal noise contribution due to integration of reference current I_{ref} and is directly proportional to the product $I_{\mathrm{ref}}T_{\mathrm{CLK}}$. Thus, decrease in I_{ref} has to be compensated by an increase in the clock period T_{CLK} to maintain a constant SNR. This results in a reduced conversion rate as has been reported in [8]. If Δ in (15) is 0 V, then SNR degrades as the reference current decreases. Addition

TABLE I
MEASURED SPECIFICATION USING THE PROTOTYPE OF MULTI-CHANNEL POTENTIOSTAT

Parameters	Values
Technology	0.5 μm 2P3M CMOS
Size	3 mm $\times$ 3 mm (42 channels)
Supply	3.3 V
Channels	42
Input Current Range	-100nA to 100nA
Resolution	10 bits
Sensitivity	50fA
Total Power dissipation	11 μW at 250KHz (1 channel)
Energy per quantization level	0.045 pJ
Active Area	0.085 mm^2 (1 channel)

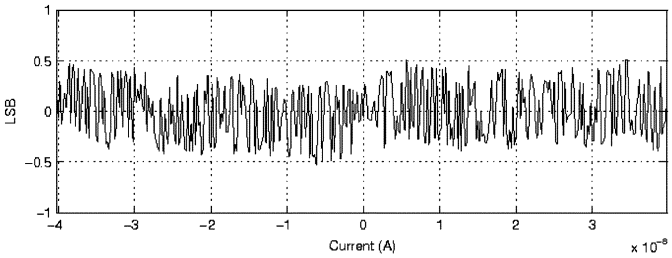

Fig. 6. Measured DNL plot for a semi-synchronous $\Sigma\Delta$ converter.

of hysteresis ensures that SNR between comparator switching cycle is atleast $(C\Delta U_T)/(4\eta KT)$, which is weakly dependent on the reference current and independent of the clock frequency. Thus, for large operational currents $I_{\rm ref}$, the SNR in (15) is dominated by conventional $\Sigma\Delta$ operation, whereas for low operational currents $I_{\rm ref}$, the SNR is determined by hysteresis levels (TEM). For 50-pA reference current, when $\Delta = 0$ V then SNR is 21.78 dB per switching cycle. The SNR improves to 38.86 and 48.78 dB per switching cycle when $\Delta = 10$ mV and $\Delta = 100$ mV respectively. This shows that for a semi-synchronous $\Sigma\Delta$ converter, noise robustness at small reference currents is ensured by using a hysteretic comparator.

The other dominant source of noise for hysteresis based converter is due to the comparator which leads to variation in parameter Δ. For the comparator shown in Fig. 5(b), the equivalent input referred noise is determined by its slew rate. The input gate capacitance of the inverter is typically small and by optimizing the value of the bias voltage $V_{\rm BIAS}$ of a comparator, the variance of Δ due to thermal noise can be effectively reduced.

V. POTENTIOSTAT CHARACTERIZATION

A prototype consisting of an array of 42 potentiostats has been fabricated in a 0.5-μm CMOS process. The size of the prototype is 3-mm $\times$ 3-mm and its micrograph is shown in Fig. 9. The active area occupied by a single semi-synchronous $\Sigma\Delta$ converter is 0.085 mm^2 which makes it one of the most area efficient potentiostat reported in the literature. Table I summarizes the specification of the multichannel potentiostat chip.

The first set of experiments were used to measure the resolution of the semi-synchronous $\Sigma\Delta$ converter. A GPIB controlled current source from *Keithley Instruments* was used to generate currents. A *digital code*, which is the output of the counter ($\sum_{n=1}^{N} D_n + \sum_{n=1}^{N_{\rm ext}} D_n^*$ in (8)) was acquired through an FPGA interface. For this experiment, the hysteresis level of the comparator was fixed to $\Delta = 100$ mV. Fig. 6 shows the measured

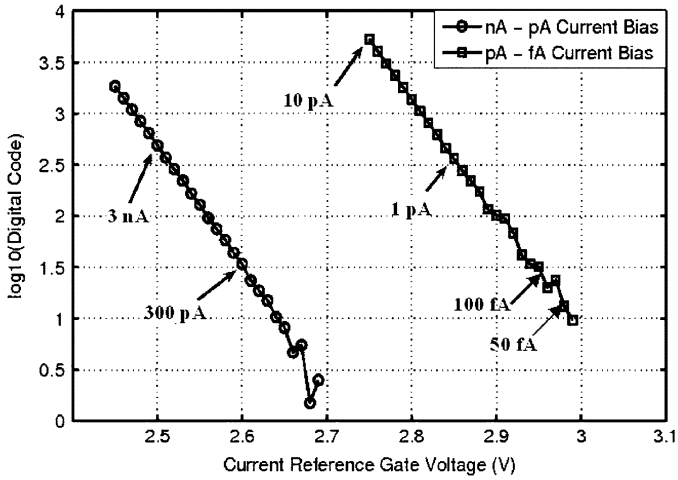

Fig. 7. Demonstration of the potentiostat for measurement of subthreshold characteristics of a pMOS transistor, whose drain current can be as low as 50 fA.

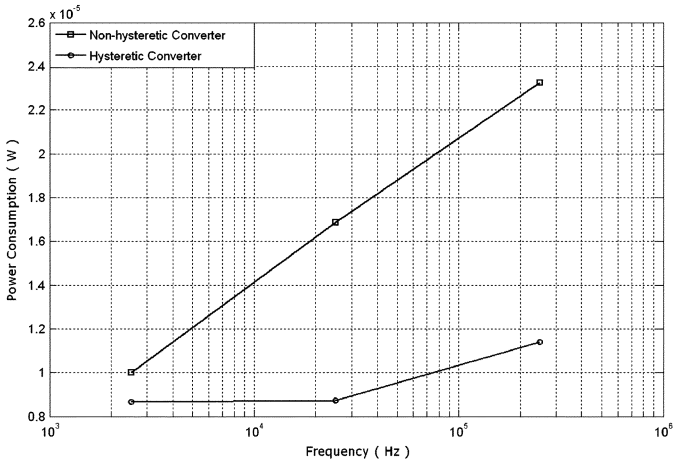

Fig. 8. Comparison of power dissipated by a semi-synchronous $\Sigma\Delta$ with a conventional $\Sigma\Delta$ for different sampling frequency.

differential nonlinearity (DNL) with the prototype potentiostat, demonstrating a resolution of 10 bits. Sensitivity measurements (minimum detectable current) was performed using an on-chip pMOS transistor with adjustable gate-to-source voltage, which has been shown to be capable of generating femtoampere range currents [21]. The use of internal current source avoids unnecessary coupling from external noise sources, which is critical for ultra-small current measurements. Fig. 7 shows a log linear plot of the digitized output produced by the semi-synchronous $\Sigma\Delta$ converter, when the gate-to-source of the pMOS transistor is varied. Landmark gate voltages were mapped onto current values using an external pico-ammeter and are indicated on the graph. Fig. 7 shows that the potentiostat can measure subthreshold currents up to 50-fA range.

Fig. 8 compares the power dissipated by the semi-synchronous converter with a conventional $\Sigma\Delta$ converter for different sampling frequencies. The plot shows that the total power consumed by prototype converter is half of the power consumed by conventional $\Sigma\Delta$ converter, with the power efficiency improving as the sampling frequency increases. This improvement can be attributed to reduced switching cycles

TABLE II
COMPARISON OF SEMI-SYNCHRONOUS $\Sigma\Delta$ WITH OTHER POTENTIOSTATS AND ADCS

	This Work	Ref. [12]	Ref. [8]	Ref. [22]
Technology(μm)	0.5	0.35	0.5	0.25
Resolution(Bits)	10.0	11.0	8	7
Sampling Rate(KHz)	250	31.25	2000	100
Power Dissipation(μW)	11.42	75	100	3.1
Energy/quantization(pJ)	0.045	1.17	0.195	0.24
Active Area(mm^2)	0.086	0.45	N/A	0.053

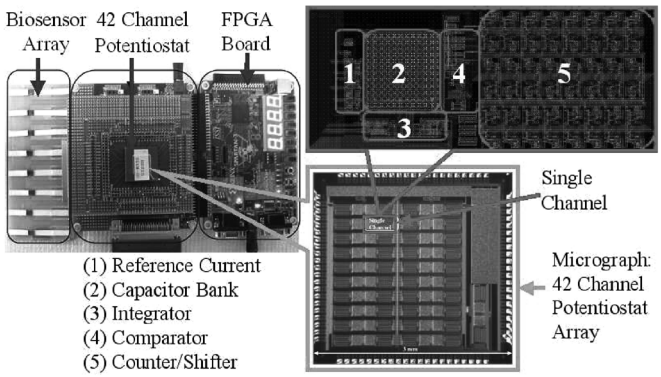

Fig. 9. Experimental setup showing the interface between biosensor array with the multichannel potentiostat.

which is controlled by the hysteresis level of a comparator. For a sampling rate of 250 kHz, the power dissipation of a single potentiostat channel is 11 μW which accounts for 8 μW consumed by the digital components and 3 μW consumed by the analog components. When compared to other reported implementations (shown in Table II), the proposed implementation of semi-synchronous $\Sigma\Delta$ converter demonstrates superior energy efficiency per quantization levels.

VI. BIOSENSOR MEASUREMENTS

We have interfaced the fabricated prototype with our previously reported multi-array biosensor [7] and have used it for measurement of conductance variations transduced by antigen-antibody binding. The model pathogen used for this experiment was *Bacillus Cereus*. Biosensors specific to *Bacillus Cereus* were fabricated, whose details can be found in [5] and are omitted here for the sake of brevity. The setup used for this experiment is shown in Fig. 9 which consists of an array of biosensors, that directly interfaces with a printed-circuit-board (PCB) hosting the multichannel potentiostat chip. A field-programmable gate array (FPGA) was used for clock generation and real-time data acquisition. Pair of potentiostats were then configured for differential conductance measurements, such that any common-mode disturbance (60-Hz coupling) at the input node is eliminated. Samples containing different concentration levels of *Bacillus Cereus* cultures were prepared and were labeled according to their dilution levels as $10^3, 10^4, 10^5$, and 10^6 colony forming units (CFU/ml). A control (Blank) solution (sample without any pathogens) was used to calibrate the response of the potentiostat. Confirmation of the pathogens followed standard microbiology protocols [23]. Counting colonies were done using the automated plater-counter in a biosafety level 2 environment. All laboratory and biohazard waste were labeled, handled, and disposed of according to the MSU standard procedures for handling biohazardous waste [24].

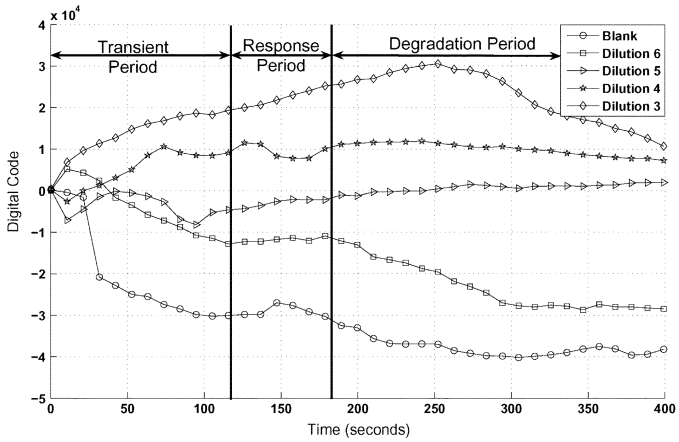

Fig. 10. Measured response of a Bacillus Cereus biosensor for different concentration levels Dilution 6: 10^6 CFU/ml, Dilution 5: 10^5 CFU/ml, Dilution 4: 10^4 CFU/ml, Dilution 3: 10^3 CFU/ml, Control Solution: Blank.

A fixed potential (100 mV) was applied across the electrodes of the biosensor, and the change in current was measured after the sample was applied to the biosensor array. Fig. 10 shows measured current for solutions with different concentration of pathogens. As shown in the figure, the response of the biosensor can be demarcated into three different periods. During the transient period (see Fig. 10), the conductance across the biosensor (hence current measured by the potentiostat) exhibits significant variations due to antibody-antigen reactions. During the response period, the conductance measurements show a stable behavior which is monotonic with the concentration of pathogens in the applied sample. During the degradation period, the biosensor response degrades due to de-hydration and due to loss of conductivity of polyaniline nanowires [5]. Thus, the three periods (epochs) in the biosensor response generate a unique signature that embeds information related to composition and concentration of pathogens in a sample. These signatures can now directly be used in the spatio-temporal method proposed in [7] for simultaneously detecting traces of multiple pathogens.

VII. CONCLUSION AND FUTURE WORK

In this paper, we introduced a novel energy-efficient semi-synchronous $\Delta\Sigma$ converter that can achieve femtoampere range sensitivity in current measurement. A multichannel potentiostat has been fabricated with the proposed architecture and its functionality has been verified for real-life biosensing application. Future improvements in implementing the semi-synchronous $\Sigma\Delta$ converter include use of comparators with accurate and digitally programmable hysteresis levels. The architecture of semi-synchronous $\Sigma\Delta$ converter can be improved by using an algorithmic conversion to implement extended counting in the compensation step. Recently, a time-encoded binary ADC was reported in [12] that can reduce the conversion time over the integrating ADC used in this paper. Another future direction will be to modulate the hysteresis levels using a digital hadamard sequence. It could therefore be possible to implement parallel semi-synchronous $\Sigma\Delta$ modulators similar to approach reported in [25].

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