Design of a Programmable Gain, Temperature Compensated Current-input Current-output CMOS Logarithmic Amplifier

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***Abstract*—This paper presents the design of a programmable gain, temperature compensated, current-mode CMOS logarithmic amplifier that can be used for biomedical signal processing. Unlike conventional logarithmic amplifiers that use a transimpedance technique to generate a voltage signal as a logarithmic function of the input current, the proposed approach directly produces a current output as a logarithmic function of the input current. Also, unlike conventional transimpedance amplifier the gain of the proposed logarithmic amplifier can be programmed using floating-gate trimming circuits. The synthesis of the proposed circuit is based on the Hart's extended translinear principle which involves embedding a floating-voltage source and a linear resistive element within a translinear loop. Temperature compensation is then achieved using a translinear-based resistive cancelation technique. Measured results from prototypes fabricated in a 0.5 μm CMOS process show that the amplifier has an input dynamic range of 120dB and exhibits a temperature sensitivity of 230 ppm/^{o}C (27^{o}C - 57^{o}C), while consuming less than 100nW of power.**

***Index Terms*—Sub-threshold analog, compression circuit, logarithmic amplifier, temperature compensation, silicon cochlea, Translinear, potentiostat.**

I. Introduction

Functionally, a logarithmic amplifier generates an output signal that is proportional to the logarithm of its input [1]. Due to the compressive nature of the $\log(\cdot)$ function, logarithmic amplifiers are useful for processing wide dynamic range signals like auditory signals whose magnitude can vary by more than 100dB. Biomedical applications of logarithmic amplifiers include: (a) signal companders in hearing aids that can be programmed to fit the hearing profile of a patient [2]; or (b) potentiostats which are required to measure electrochemical currents ranging from a few fA to 100nA [3]–[5]. In literature, logarithmic amplifiers have also been used in cochlear implants [6], [7] and in silicon cochleas [8], [9] where the logarithmic compression has been used for computing the cepstrum of an auditory signal.

The most popular method for implementing logarithmic amplifiers is the transimpedance-based approach that exploits the exponential dependence between the current and the voltage across a p-n junction diode [10], a bipolar transistor [11] or a MOSFET biased in weak-inversion. Using this approach, amplifiers with input dynamic range greater than 100dB have been reported [12]. However, there are two main disadvantages of the transimpedance-based method: (a) the gain of these amplifiers are static and are generally determined by the sub-threshold slope of the MOSFET; (b) due to their dependence on the current-to-voltage relationship, these amplifiers are sensitive to temperature variations and therefore require additional and complex compensation circuitry; and (c) for current-mode analog signal processing, the use of transimpedance-based logarithmic amplifiers requires additional transconductance stages to convert the output voltage into useful currents [10].

In this paper we present the design of a current-input, current-output logarithmic amplifier, which by design is insensitive to variations in temperature. At the core of the proposed design is an extended translinear principle proposed by Hart [13] which exploits embedding of floating-voltage sources and linear resistive elements within a translinear loop [14]. By introducing additional translinear loops, temperature compensation is achieved through a resistive cancelation technique. In this paper, we analyze the performance of the logarithmic amplifier and verify its functionality using measured results from a fabricated prototype. The gain of the proposed amplifier can be programmed using floating-gate trimming circuits and the input to the proposed amplifier can be programmed using a digitally addressable current-mode DAC. The paper is organized as follows: section II briefly presents the extended translinear principle which is then used to describe the operational principle of the basic logarithmic amplifier. Section III presents a complete circuit level implementation of the proposed logarithmic amplifier including the programming, temperature and trimming/calibration circuits. Section IV describes the measured results obtained from prototypes fabricated in a 0.5μm CMOS process and section V concludes the paper with a brief discussion on the measurement results, future directions and challenges.

II. Logarithmic Computation based on Extended Translinear Principle

The translinear principle [11] exploits the exponential relationship between voltages and currents in certain devices (diodes, BJTs and sub-threshold MOSFETs) and the principle has been successfully used for implementing analog signal processors [15], [16]. The proposed logarithmic amplifier is based on an extension of the translinear principle proposed by Hart [13] and exploits embedding of arbitrary voltage sources within a translinear loop. The design principle is explained using an example circuit shown in Fig. 1 which

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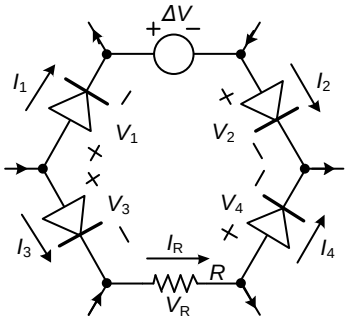


Fig. 1. Illustration of extended translinear principle.

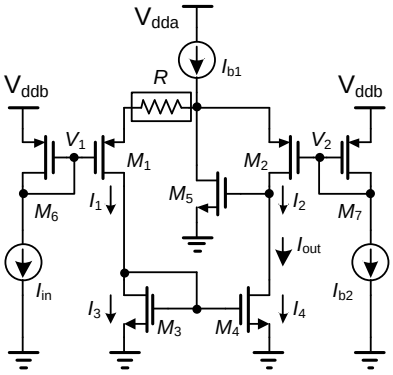


Fig. 2. Basic current-input current-output logarithmic amplifier.

consists of several diodes $D_{1\text{–}4}$ acting as translinear elements connected to a floating-voltage source ΔV and a memoryless, linear resistive element R. The linear resistor models relationship between the current (I_R) flowing through R and the voltage (V_R) across R according to

$$I_R = \frac{V_R}{R}. \tag{1}$$

If the voltage drop across each of the diodes in Fig. 1 is denoted by $V_{1\text{–}4}$ then,

$$V_1 + V_2 + \Delta V = V_3 + V_4 + V_R, \tag{2}$$

which after using the diode equation $I_{1\text{-}4} = I_s \exp\left(V_{1\text{-}4}/U_T\right)$ leads to the Hart's formulation [13],

$$I_1 \cdot I_2 \cdot \exp\left(\frac{\Delta V}{U_T}\right) = I_3 \cdot I_4 \cdot \exp\left(\frac{V_R}{U_T}\right), \tag{3}$$

and hence,

$$V_R = \Delta V + U_T \log\left(\frac{I_1 \cdot I_2}{I_3 \cdot I_4}\right) \tag{4}$$

$$I_R = \frac{\Delta V}{R} + \frac{U_T}{R} \log\left(\frac{I_1 \cdot I_2}{I_3 \cdot I_4}\right). \tag{5}$$

U_T in equations (3) and (5) refers to the thermal voltage which is linearly proportional to the absolute temperature and is approximately equal to 26mV at room temperature (25°C).

Equation (5) is now applied to the basic MOSFET circuit shown in Fig. 2. The circuit is derived from a previously reported translinear circuit [16] where the transistors M_1,M_2,M_6 and M_7 are biased in weak-inversion and form a translinear loop. The drain-to-source voltages for all transistors can be assumed to be greater than 100mV, in which case the transistors satisfy the following exponential relationships [17]:

$$NMOS: I_n = S_n I_{D0n} e^{(V_{Gn} - V_{Tn})/n_n U_T} e^{-V_{Sn}/U_T}, \tag{6}$$

$$PMOS: I_p = S_p I_{D0p} e^{(-V_{Gp} + V_{Tp})/n_p U_T} e^{V_{Sp}/U_T}, \tag{7}$$

The parameters $S_{n,p}$, $V_{Tn,p}$, $n_{n,p}$, U_T, $V_{Gn,p}$, and $V_{Sn,p}$ denote the aspect ratio, the threshold voltage, the sub-threshold slope, the thermal voltage, the gate and the source voltages which are respectively referred to the bulk potential of their respective transistors (V_{dd} for a pMOS transistor and gnd for an nMOS transistor). The transistor M_5 serves as a feedback element which clamps the voltage at the drain of M_2 as a function of the current I_{b2}. If the aspect ratios of the transistors are assumed to be equal, the current mirror formed by M_3 and M_4 ensures $I_{out} = I_1 = I_2$. Then, using equation (5) on the extended translinear loop formed by M_1,M_2,M_6,M_7 and the resistor R, the output current I_{out} can be expressed as

$$I_{out} = \frac{U_T}{R} \cdot \log\left(\frac{I_{in}}{I_{b2}}\right). \tag{8}$$

Thus, the output current I_{out} is proportional to the logarithm of the current I_{in}. Note that $I_{in} > I_{b2}$ for the circuit to be operational. Also, note that the circuit in Fig. 2 uses two different supply voltages V_{dda} and V_{ddb} with $V_{dda} > V_{ddb}$ to ensure that the current source I_{b1} has a sufficient voltage headroom to operate. The DC response of the circuit in Fig. 2 has been simulated and the results are shown in Fig. 3. The result plots the output current I_{out} for different aspect ratios

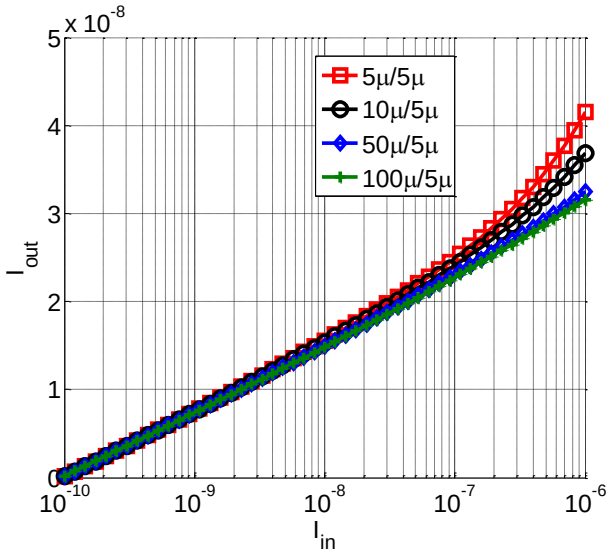


Fig. 3. Simulated DC response illustrating the effect of different transistor aspect ratios for the circuit shown in Fig. 2

of the pMOS transistors (shown in the figure legend) as the input current I_{in} is varied from 100pA to 1μA. For this simulation, the bias current I_{b2} was chosen to be 100pA and the resistance R was set to 10MΩ. The result shows that as long as the transistors are biased in weak-inversion, the response of the circuit in Fig. 2 is indeed logarithmic as described by equation 8. The simulation result also shows that the input dynamic range of the basic circuit can be extended by using transistors with larger aspect ratios. However, the use of larger transistors adversely affects the response time of the amplifier, in particular when the magnitude of the input current is small. Equation (8) consists of several temperature dependent parameters which includes: (a) the thermal voltage U_T; and (b) the resistance R. Fortunately, all the parameters affect only the gain of the amplifier and hence can be canceled according to the procedure described in the next section.

III. Compensated Programmable Logarithmic Amplifier Circuit

Fig. 4 shows the schematic of the temperature compensated logarithmic amplifier. It consists of an input stage A_1, a reference stage A_2 and a translinear stage A_3. The input stage and the reference stage is formed using the basic circuit shown in Fig. 2. Based on equation (8), the output current I_x generated by the input stage I_{in} is given by

$$I_x = \frac{U_T}{R} \cdot \log\left(\frac{I_{in}}{I_{b2}}\right). \tag{9}$$

For the reference stage A_2 the ratio of the currents I_1 and I_2 is set to 2 using the current mirrors. Thus, using equation (8) the reference current I_{ref} is given by

$$I_{ref} = \frac{U_T}{R} \cdot \log(2) \tag{10}$$

$$I_{ref} = 0.693 \cdot \frac{U_T}{R}. \tag{11}$$

The translinear stage A_3 consists of a translinear loop formed by the pMOS transistors M_9-M_{12}, which leads to $I_{out} \cdot I_{ref} = I_{b4} \cdot I_x$. Note that I_{b1} in Fig. 4 is an external bias current required to establish the translinear loop and it's magnitude is generally chosen to be 10 times larger than I_{b4}. M_{15} is added at the input of I_{b4} to ensure M_{11} is always in saturation. Applying the translinear principle to the transistors M_9-M_{12} and after applying equations (9) and (11), the output current I_{out} can be expressed as

$$I_{out} = I_{b4} \cdot \frac{I_x}{I_{ref}}$$

$$I_{out} = 1.44 \cdot I_{b4} \cdot \log\left(\frac{I_{in}}{I_{b2}}\right). \tag{12}$$

If the currents I_{b4} and I_{b2} are assumed to be invariant to temperature variations, I_{out} is also theoretically invariant to temperature variations. The current I_{b4} determines the gain of the amplifier and the current I_{b2} determines the lower bound on the input current I_{in} of the amplifier.

The circuit in Fig. 4 requires that the current sources I_{b2} and I_{b4} be calibrated to different amplifier settings. It turns out that the core circuit shown in Fig. 2 can also be used for designing a programmable current reference as shown in Fig. 5(a). If the gate voltages of M_{fg1} and M_{fg2} are denoted by V_{G1} and V_{G2}, then the current I_{out} in Fig. 5(a) can be expressed as $I_{out} = (V_{G1} - V_{G2})/R$. If the resistance R is temperature compensated and the voltage difference $V_{G1} - V_{G2}$ is independent of temperature then I_{out} will also be temperature compensated. Note that once I_{out} is generated on-chip, different current levels can be generated using current mirrors. On-chip temperature compensation of the resistor in current references is described elsewhere [18] and is omitted here for the sake of brevity. The voltages V_{G1} and V_{G2} in Fig. 5(a) are generated respectively using a programmable floating-gate voltage reference which has been reported in [19]. If the floating-gate transistor M_{fg1} is matched to the current source transistor M_1, the output voltage V_{G1} is given by

$$V_{\mathrm{G1}} = V_{\mathrm{dd}} - nV_{\mathrm{b1}} + n\frac{Q_1}{C_{\mathrm{T}}}, \tag{13}$$

where n is the sub-threshold slope factor, V_{dd} and V_{b1} is the supply and biasing voltages. Q_1 in equation (13) represents the charge on the floating-gate F_1 and C_{T} is the total capacitance at nodes F_1 and F_2. Thus

$$V_{\mathrm{G1}} - V_{\mathrm{G2}} = n\frac{Q_1 - Q_2}{C_{\mathrm{T}}}, \tag{14}$$

where Q_2 is the charge on the floating-gate F_2. The charges Q_1 and Q_2 are programmed using a linear injection technique [19], where the opamps A_1 and A_2 implement an active feedback that maintains the source, gate and drain voltages of M_{fg1} and M_{fg2} constant. The feedback circuit alleviates any non-linear artifacts in the hot-electron injection process, thus achieving a stable and controllable injection of electrons onto the floating-gate. For the sake of brevity, we have omitted details of hot-electron injection programming which can be found in [19]. When calibrating the current-reference in Fig. 5, the voltage V_{G2} is first programmed to a common-mode value by periodically enabling the active feedback loop using the switch S_P. V_{G1} is programmed in a similar fashion, however, the output current I_{out} is monitored after each programming cycle. The calibration procedure ends when the output current reaches the desired value. Fig. 7 shows an experimental result which shows that the output current can be linearly programmed with an accuracy of $\pm 0.7\%$.

Programming of the input current I_{in} is achieved using a 10-bit current-mode DAC shown in Fig. 5(b). The architecture of the current DAC is based on a resistive divider topology [20], where the current through each branch is recursively divided by a factor of two. The bits d_{10}–d_1 determine the binary weighted sum of the current which is then mirrored into the input stage. A serial shift register chain is used for programming the bits d_{10}–d_1 using an FPGA. The DAC is calibrated post-fabrication and the mapping between the bits d_{10}–d_1 and the input currents are stored offline.

IV. Measurement Results

The proposed logarithmic amplifier has been prototyped in a 0.5μm standard CMOS process and Fig. 6 shows the micrograph of the fabricated prototype. Table I summarizes

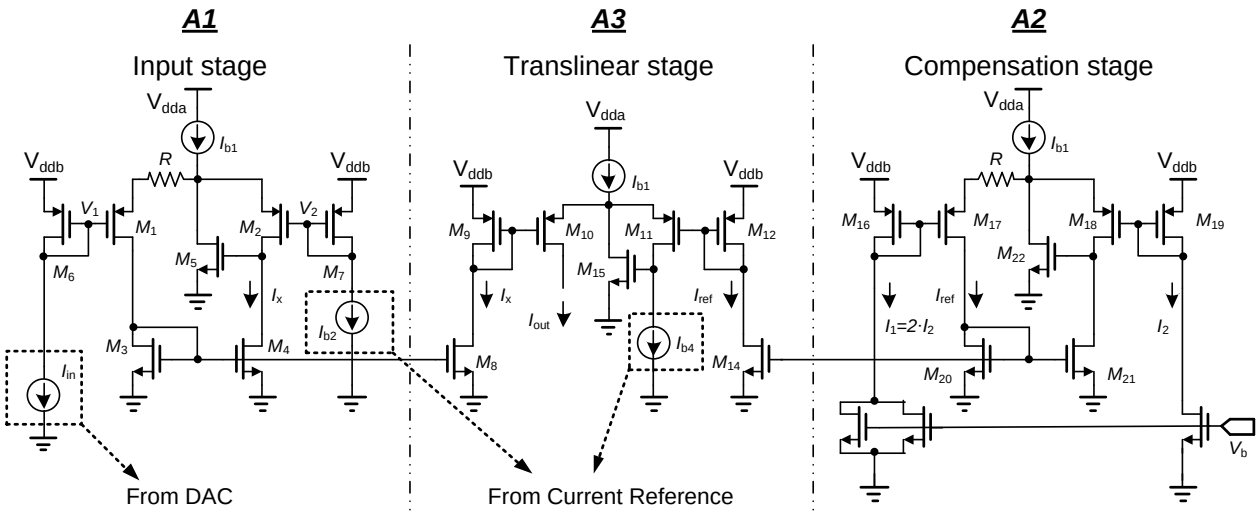


Fig. 4. Complete schematic of the temperature compensated programmable logarithmic amplifier.

different circuit parameters that have been used for the design of the amplifier.

TABLE I
CIRCUIT PARAMETERS USED FOR DESIGNING THE LOGARITHMIC AMPLIFIER

Fabrication Process	Standard CMOS $0.5\mu m$
Die Size	$3000\mu m \times 3000\mu m$
$M_{1\text{-}4,\,6\text{-}7}$ (refer to Fig. 2)	10μm/5μm
M_5 (refer to Fig. 2)	30μm/1.5μm
R (refer to Fig. 2)	10MΩ

A. DC Response of the logarithmic amplifier

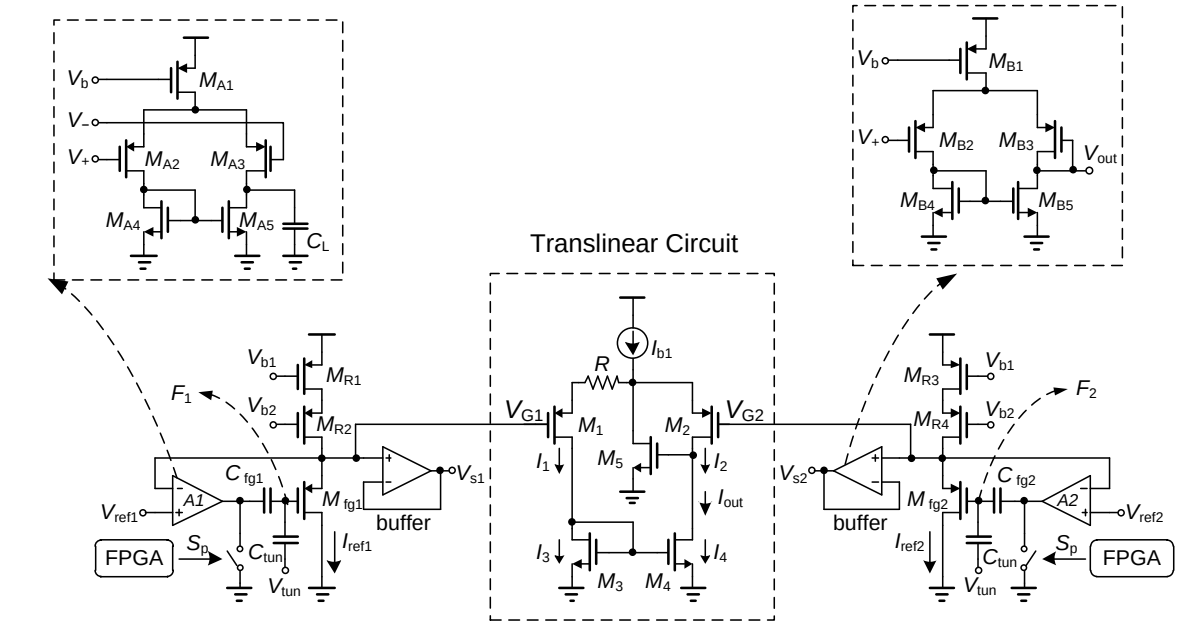
The first set of experiments measured the DC response of the logarithmic amplifier. The input current was varied from 100pA to 40nA (within the weak-inversion region of the transistor) for different settings of I_{b4}. Even though the proposed logarithmic amplifier can operate over the entire sub-threshold range of currents (typically 100fA to 100nA), the input dynamic range of the amplifier is determined by the resolution of the input current DAC, which for this design is 10 bits. The measured results are shown in Fig. 8 where the output current is plotted on a linear scale (Fig. 8(a)) and on a log-linear scale (Fig. 8(b)). The results show that the response of the logarithmic amplifier closely approximates the ideal response as given by equation (12). The results also shows that the current I_{b4} can be used to control the gain and hence the output range of the logarithmic amplifier. Fig. 8 (c) plots the residual error after a log-linear regression is performed on the experimental data. The residue plot reveals second order effects in the amplifier response which is primarily attributed to the non-linear response of the input current DAC. Also, at lower magnitudes of current (in fA), many of the conventional circuit topologies (like current mirrors) saturate as the gate-to-source voltage can not be significantly reduced below the threshold voltage [21].

B. Transient response and bandwidth

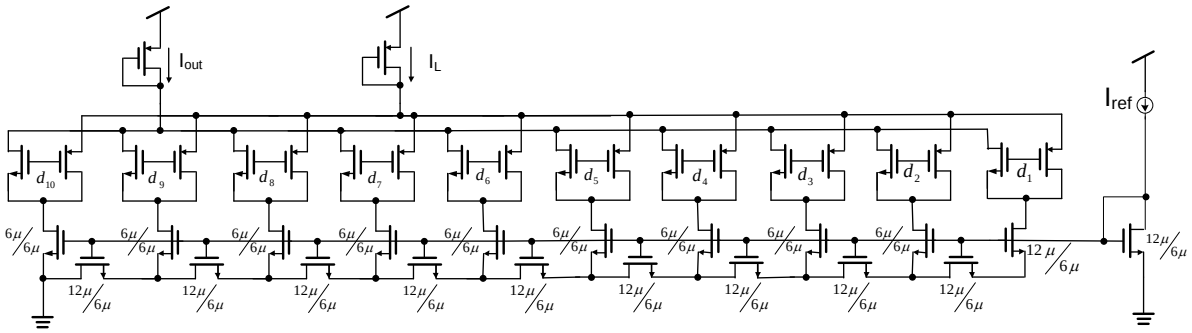
By definition, a logarithmic amplifier is a non-linear system. Therefore, the frequency response of a logarithmic amplifier has meaning only under small-signal operating conditions. However such an analysis is useful for gaining insight into the dynamic response of the amplifier. For the core circuit shown in Fig. 2, the role of the common-source amplifier formed by the transistor M_5 and the current-source I_{b1} is critical to the transient behavior of the amplifier.

M_5 ensures that I_2 can be set to very low-current values without significantly affecting the location of the pole at the source node of M_2. Thus, the transient response of the core circuit shown in Fig. 2 will be determined by the transient response of the input-stage formed by M_1 and M_6 and by the current mirror stage formed by M_3 and M_4. This in-turn is determined by the small-signal transconductance g_m of the transistors M_1, M_6, M_3 and M_4. The transient response of the complete amplifier shown in Fig. 4 will also be determined by poles located at gates of M_9 and M_{12}, all of which are located along the signal path.

To estimate the equivalent bandwidth of the system, we measured the step-response of the system and then computed the equivalent rise-time, assuming that the logarithmic amplifier behaves as a single-pole system. For this experiment, a step input is applied to I_{in} and I_{b4} whereas I_{b2} is fixed to be 100pA. A standard transimpedance amplifier circuit (formed by a resistor connected across the output and inverting terminal of a COTS opamp) was used and the output of this amplifier was monitored when a step-input was applied to the current parameters I_{in} and I_{b4}. Fig. 9(a) shows a



(a)



(b)

Fig. 5. Programming and trimming circuits:(a) floating-gate current reference; and (b) current DAC.

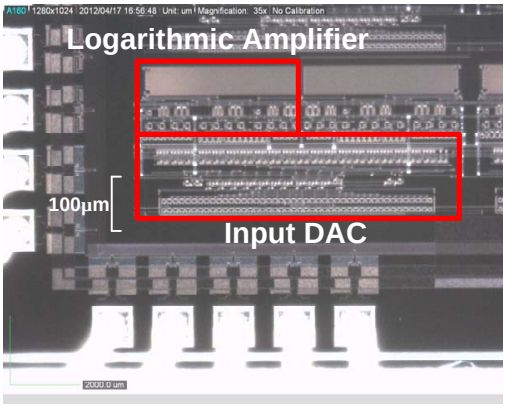
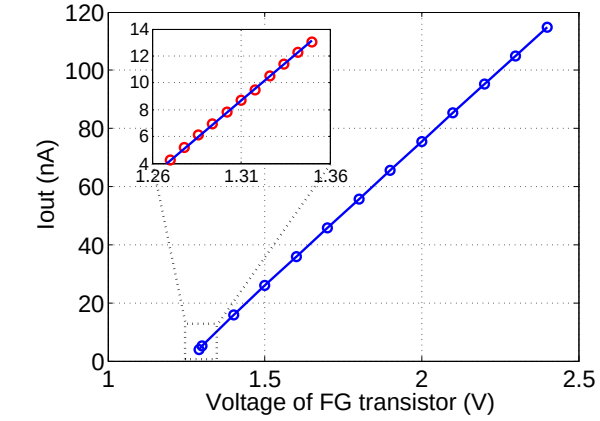


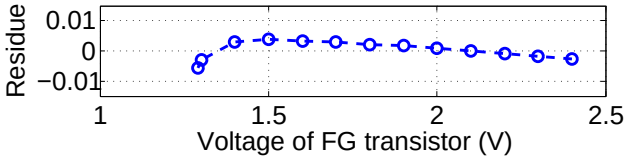
Fig. 6. Die microphotograph of the logarithmic amplifier.

sample of the result when I_{in} was changed from 49nA to 110nA while I_{b2} was set to 100pA and while I_{b4} was set to 380pA and 750pA respectively. Note that because the logarithmic amplifier is non-linear, the rise-time and fall-time measurements could potentially be different. For our results, we chose the maximum of the rise-time and fall-time for bandwidth computation.

Fig. 9(a) shows the approximate bandwidth when the input current is varied from $49nA$ to $110nA$, keeping the current step-size constant. The result shows that the bandwidth of the amplifier remains constant as I_{in} is increased up to a certain threshold, after which the bandwidth increases monotonically. When the magnitude of the input current is small the bandwidth is determined by the tail current of the common source amplifier I_{b1}, which for this experiment is held constant. For I_{in} greater than the tail current I_{b1}, the bandwidth now becomes proportional to I_{in}. Fig. 9(b) shows the approximated bandwidth when I_{b4} is varied. For larger values of I_{b4}, the bandwidth remain approximately constant because the transient behavior of the signal path formed by M_1 to M_7



(a)



(b)

Fig. 7. (a) Measurement output current as the floating-gate voltage is programmed; and (b) Residue computed as the ratio of programming error and the programming current, showing that the error in programming is less than $\pm 0.7\%$.

is determined by I_{b1}. At smaller values of I_{b4}, the transient response is determined by how fast the gate of M_{15} can be charged, and hence the bandwidth reduces monotonically. All the measured results show that for sub-threshold biasing and for the given sizes of the transistors, the maximum bandwidth was estimated to be 1.2KHz. Fig. 9 (c) shows the estimated bandwidth when I_{b1} is varied. For this experiment, I_{in} is fixed at 92nA, and all the other biasing current were constrained to ensure sub-threshold operation. The result shows that the bandwidth of the amplifier increases when I_{b1} is increased and I_{b1} controls the maximum bandwidth of the amplifier.

C. Noise Measurements

Given the non-linear response of the logarithmic amplifier, an extensive noise-analysis of even the basic circuit shown in Fig. 2 is complicated. For the following noise-analysis we will assume that all sources of noise are thermal in nature, keeping in mind that similar analysis can also be performed for flicker-noise. The sources of noise for the logarithmic amplifier are shown in Fig. 10 where the MOSFET noise has been referred to the gate-terminals of their respective transistors. In this analysis, it is also assumed that the input current is noisy with the noise current denoted by a random variable $I_{in,n}$, as shown in Fig. 10. A straight-forward way to estimate the noise in the output current is to realize that all the gate-referred noise voltages are floating-voltage sources in the translinear loop as shown in Fig. 10. Therefore, using the extended translinear principle the variance of the output noise current $I^2_{out,n}$ due to the noise sources $V_{M1,n}$,$V_{M2,n}$,$V_{M3,n}$,$V_{M4,n}$, $V_{R,n}$ and $I_{in,n}$ is given by

$$\begin{aligned} I^2_{out,n} &= \frac{V^2_{M1,n} + V^2_{M2,n} + V^2_{M3,n} + V^2_{M4,n} + I^2_{in,n}/g^2_m}{R^2} \\ &= \alpha \frac{KT}{g_m R^2} + \frac{4KT}{R} + \frac{I^2_{in,n}}{g^2_m R^2} \end{aligned} \quad (15)$$

where K is the Boltzmann's constant and T is the temperature. Note that in our analysis we have assumed that the small signal transconductance of all the transistors equals g_m and all noise sources are mutually uncorrelated. Also the parameter α is a constant and is a function of the number of MOS transistors and their biasing conditions. To measure the output noise current, we first fixed the signal-to-noise ratio (SNR) of the input current at 50dB as shown in Fig. 11(a). Therefore, the variance of the input noise can be expressed in terms of the magnitude of the input current I_{in} as $I^2_{in,n} = I^2_{in}/SNR$. Thus, using equation (15), the magnitude of the output noise current can be written as

$$I_{out,n} = \left(\alpha \frac{KT}{g_m R^2} + \frac{4KT}{R} + \frac{I^2_{in}}{(SNR) g^2_m R^2} \right)^{1/2}. \quad (16)$$

Note that for the temperature compensated logarithmic amplifier shown in Fig. 4, the output current I_{out} will be scaled by the gain of the translinear stage A3, however, the trend with respect the magnitude of the input current will remain unchanged. Fig. 11(b) shows the measured output noise current (over a bandwidth of 4KHz) as the input current is varied.

D. Temperature Measurement and Compensation

The extended translinear principle implicitly leads to a logarithmic amplifier that is temperature compensated. According to equation (12), the temperature dependence of I_{out} is determined by the temperature characteristics of I_{b4}, I_{b2}, and I_{in} and can be expressed as

$$I_{out}(T) = 1.44 I_{b4}(T) \cdot (\log(I_{in}) - \log(I_{b2}(T))). \quad (17)$$

where each current reference is assumed to be a function of the temperature T. Since temperature compensation of current references have already been reported [18], the objective of the experiments presented in this section is to verify that the logarithmic function can be implemented in a temperature insensitive manner. Therefore, we use an external temperature compensated current source to generate the input current I_{in}, where as the temperature dependent terms in equation (17) is eliminated by using a bilinear measurement technique.

If $I_{out_1}(T), I_{out_2}(T)$ and $I_{out_3}(T)$ are the output currents corresponding to three different values of the input currents I_{in_1}, I_{in_2} and I_{in_3}, measured at a fixed temperature T, then the following bilinear transformation is obtained:

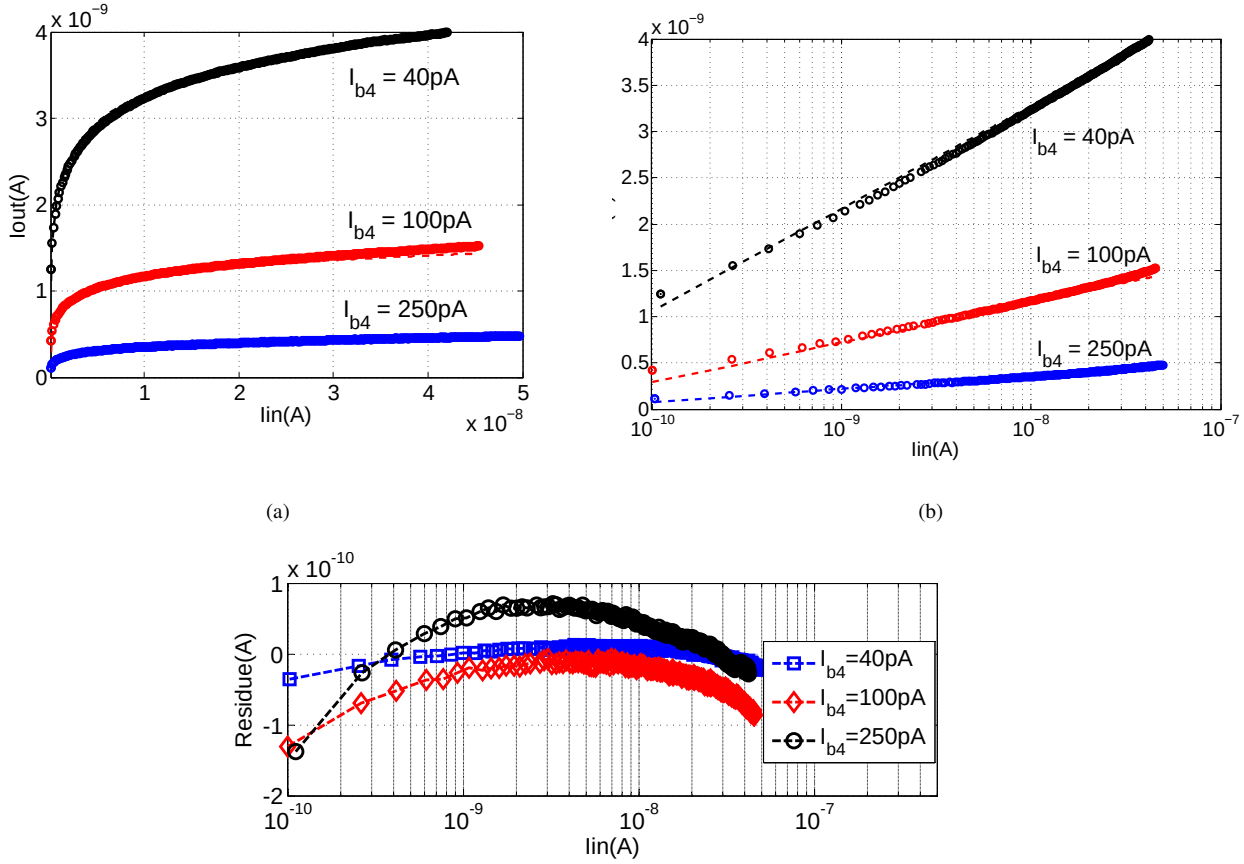


Fig. 8. Measured DC response: (a) and (b) showing logarithmic relationship between the input and output current; (c) residue illustrating deviation from the ideal logarithmic response.

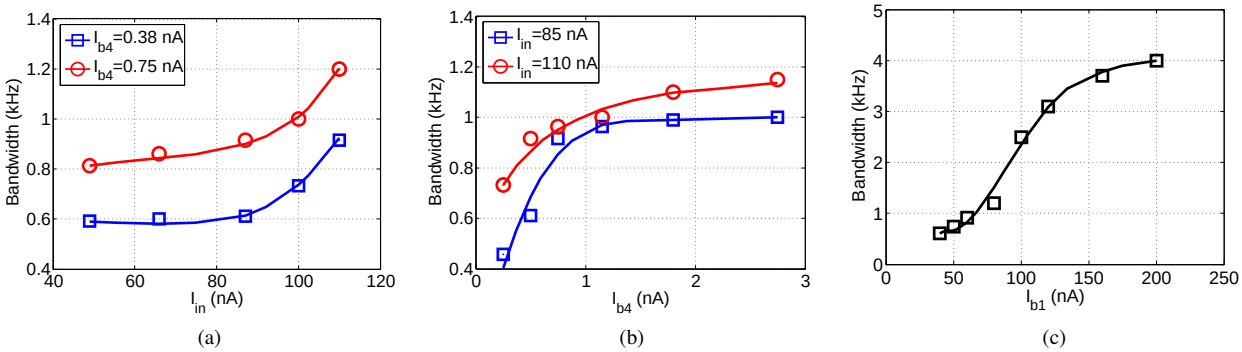


Fig. 9. Estimated bandwidth of the logarithmic amplifier when: (a) I_{in}; (b) I_{b4}; (c) I_{b1} is varied.

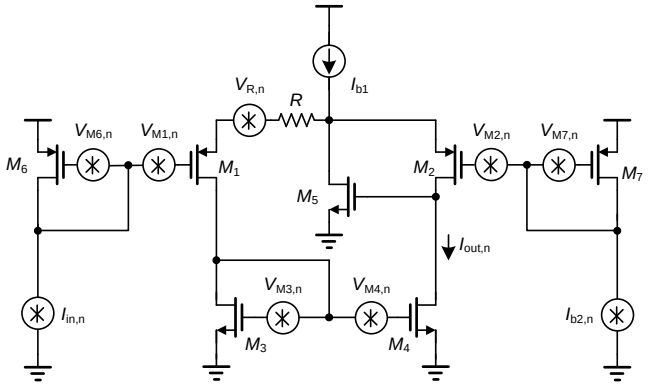


Fig. 10. Schematic showing sources of noise in the core logarithmic amplifier

$$\frac{I_{out_1}(T) - I_{out_2}(T)}{I_{out_1}(T) - I_{out_3}(T)} = \frac{\frac{I_{b4}(T)}{\log 2} \cdot \log\left(\frac{I_{in_1}}{I_{in_2}}\right)}{\frac{I_{b4}(T)}{\log 2} \cdot \log\left(\frac{I_{in_1}}{I_{in_3}}\right)} = \frac{\log\left(\frac{I_{in_1}}{I_{in_2}}\right)}{\log\left(\frac{I_{in_1}}{I_{in_3}}\right)} \quad (18)$$

It can be seen from the equation (18), that the bilinear transformation is only a function of the logarithmic function of the input, where as all the temperature dependent terms due to the current references are canceled. Thus, if the proposed amplifier is indeed temperature compensated, then the bilinear measurement should in principle be temperature compensated.

For the next set of experiments, the device under test was placed in a programmable temperature chamber and the temperature was varied from 27^oC to 57^oC. For each temperature setting, the input current is set to three pre-set values and the corresponding output current and the bilinear expression is computed according to equation (18). The experimental results are shown in Fig. 12 which shows that the bilinear expression is temperature compensated. Based on this measurement, the temperature sensitivity was calculated to be 230 ppm/^{o}K as shown in the Fig. 12(inset).

V. Conclusions

In this paper we have presented the design of a current-input, current-output logarithmic amplifier circuit for low-power sensory signal processing applications. The circuit is based on an extended translinear principle which requires embedding a floating voltage source and a linear resistive element within a translinear loop. Temperature dependence and circuit non-linearity is compensated using additional translinear loops and by using programmable current references. When compared with other logarithmic amplifiers that have been reported for similar applications, the proposed architecture is unique as is summarized in Table II. The current-input, current-output topology enables the proposed amplifier to have a wide output dynamic range that can be programmed using different biasing parameters. In comparison, the output dynamic range of a current-input voltage-output amplifier is limited by the supply voltage range. Also, the proposed amplifier is temperature compensated where as temperature compensation of current-input voltage-output topology is generally considered to be difficult. Other performance metrics shown in Table II are comparable and is determined by the specifications desired by an application. We would like to point out that there exist a different class of logarithmic amplifiers for microwave applications [25], [26], we have not included in the table of comparison. The reason being, that these amplifiers are designed using non-CMOS processes and specifically for radar processing with power budgets ranging from hundreds of milli-watts to a few watts.

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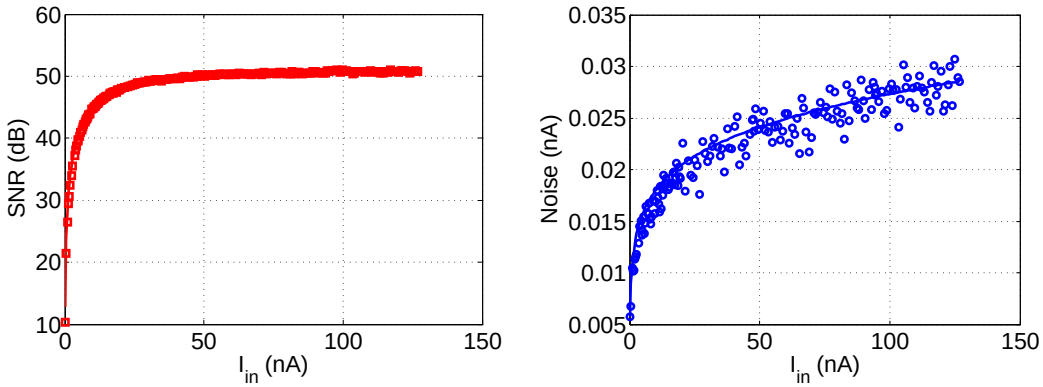

(a) (b)

Fig. 11. (a) Measured SNR of the input current I_{in}; and (b) Measured output current noise δI_{out} when I_{in} is varied.

TABLE II
COMPARISON OF PERFORMANCE

Reference	[22]	[23]	[24]	[12]	This work
Conversion	current-in voltage-out	current-in voltage-out	current-in voltage-out	current-in voltage-out	current-in current-out
Process	$1.6\mu m$	$1.5\mu m$	Discrete	$0.5\mu m$	$0.5\mu m$
Area	-	$2.9 \times 3.7mm^2$	-	$91 \times 75\mu m^2$	$290 \times 140\mu m^2$
Supply	-	$\pm$ 6 V	-	3.3 V	3.3 V
Bandwidth	>10Hz	1kHz	25kHz	>3.5kHz	4kHz
Power	10pA-1μA	30mW	-	0.1μW-33μW	1nW-10μW
Temperature Compensation	None	None	None	None	230ppm/^{o}K

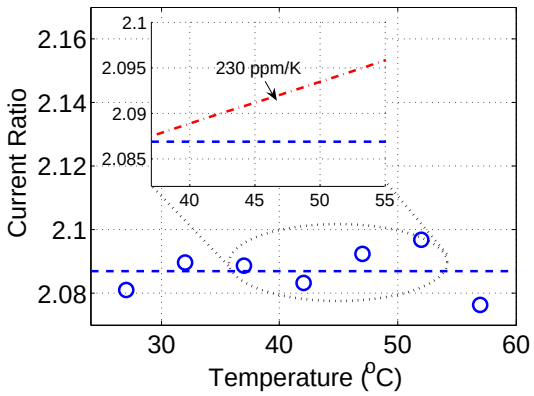

Fig. 12. Measured response showing $\frac{I_{out_1}(T) - I_{out_2}(T)}{I_{out_1}(T) - I_{out_3}(T)}$ under different temperatures.

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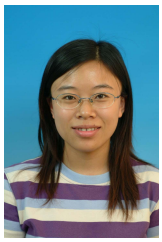

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